DD48
Dynamic Digital Subsystem

AEROFLEX
A passion for performance.

AXIe Compatible Instrument with 48 Flexible Digital Channels

Pattern Generator Features

- 32 M unrestricted (128 M, SMMode) vector memory
- 3 unique 1G SCAN chains per board
- 128 M digital sample source/capture memory
- Match mode, parallel and serial
- Industry standard pattern micro-instructions
- Flexible mixed signal triggering
- Synchronization between DD48 boards

Timing and Formatting Features

- 100/200/400 MVec/S data rates
- 32 per pin flexible edge sets, 40 ps resolution
- 32 period sets (10 ns to 671 mS periods, 40 fs accuracy)
- 127 global timing sets on-the-fly
- Window and strobe compare formats
- Flexible drive formats for mixed-signal applications
- 4 flexible edges per pin for unique formats

Driver, Comparator and Load Features

- 3 level driver (Vih, Vil, Vtt)
- -2 v to +6.0 v Range
- Active load up to 12 mA source and sink
- 1 high voltage driver (12 v) per 8 pins

Per Pin PMU Features

- Force V, Measure I; Force I, Measure V
- Voltage clamps
- 5 current ranges (2 uA to 32 mA)
- -2 v to +6.0 v range
- Hardware measurement averaging

Applications

- Digital dominant mixed signal, SOC
- Characterization, wafer sort and final test
- Multi-site, low overhead product solutions

General Description

The DD48 is a self contained single slot AXIe 3.1, 48 channel mixed-signal digital subsystem. Refer to Figure 1. Each DD48 has an independent sequencer controller with pattern generators, and an independent per channel timing system. Integrated timing generators connect directly to the instrument's pin electronics. Each pin card can operate independently or synchronously with other DD48 cards. Each pin can drive and compare data up to 400 MVec/S.

Each group of 8 channels can operate independently in terms of PMU measurements, digital sample source/capture, SCAN, and channel configuration. For example, the PMU measurement hardware supports native averaging across all pins, and 6 pins can be measured in parallel. Also, SCAN can be sourced simultaneously on some pins while digital sample source/capture occurs on other pins. All this increases test efficiency and lowers cost of test.

Each DD48 has 6 digital sample source engines and 6 digital signal capture engines. Each engine can operate independently across 8 channels or be grouped together to form a larger source or capture segment for bigger busses. Each source and capture engine can be configured to operate in serial mode (LSB or MSB first). Each engine also has access to 128 MB of memory, shared between one source and one capture engine, providing ample storage capability.

As part of the AXIe standard, each DD48 has Intelligent Platform Management, or a built in monitoring system, for the measurement of board voltage levels, device temperatures, general board temperature and FRU EEProm. A native PCI Express (PCIe) subsystem supported by the AXIe standard provides up to 100 MB/s throughput to the DD48.

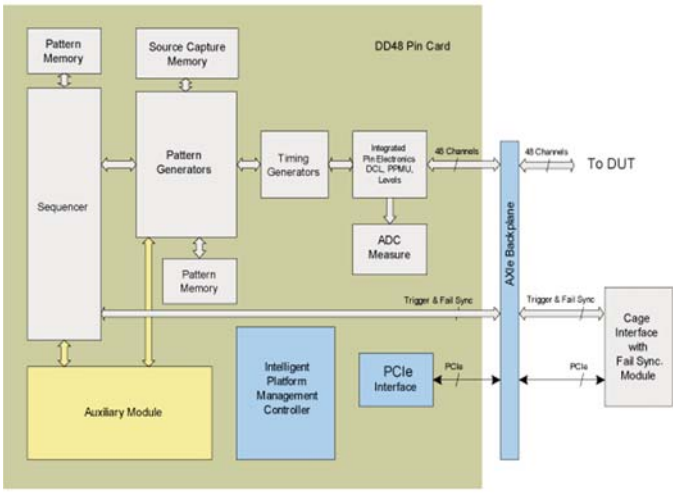

Figure 1. DD48 Block Diagram

Timing and Formats

DD48 timing architecture provides an on-the-fly selection of 127 timing sets. A timing set specifies 1 of 32 global period sets and a per pin edge set. A global period set map is used to map the 127 possible timing sets to 32 on-the-fly period sets during pattern execution. The per pin edge set map is used to assign 127 possible timing sets to one of the following:

- 32 on-the-fly edge sets when in Quad Marker Mode (QMM)
- 4 on-the-fly edge sets when in Dual Marker Mode (DMM)
- 1 edge set when in Single Marker Mode (SMM)

Clock Generation

The digital subsystem clock source (100 MHz) and can be phase locked to an external 10 MHz reference.

Period Generation

The period generator has up to 32 period sets which can be changed on-the-fly during pattern execution. Each period set consists of a T0 period duration and an integer number of C0 periods to be sourced during the T0 period. The minimum period for T0 and C0 is 10 ns.

Each channel can be referenced to either the T0 or the C0 cycle. The T0 cycle is the default reference cycle for all channels and represents the base vector rate for sequencer instructions while the C0 cycle allows clock channels to operate at a higher rate than data channels. Channels referenced to the C0 cycle must be drive only.

Each channel can be configured in one of three marker modes: Quad Marker Mode (QMM), Dual Marker Mode (DMM) and Single Marker Mode (SMM). The DUT period and T0 Period is described below for each of the marker modes:

T0/C0 Frequency Range	**1.5 Hz to 100 MHz**	**Edge placement limited to 163.8 uS**
DUT Data Rate		
QMM	100 MVec/S Max.	Equal to T0 Frequency
DMM	200 MVec/S Max.	Equal to 2 times T0 Frequency
SMM	400 MVec/S Max.	Equal to 4 times T0 Frequency
T0/C0 Period Range	10 nS to 671 mS	Edge placement limited to 163.8 uS
T0 Period Resolution	39 fS (10 nS/218)	
DUT Period		
QMM	10.0 nS Min.	Equal to 100% of T0 Period
DMM	5.0 nS Min.	Equal to 50% of T0 Period
SMM	2.5 nS Min.	Equal to 25% of T0 Period
Number of Period Sets	32	

Edge Generation

Timing Generators per Channel (QMM) 100 MVec/S

A channel configured in QMM has up to 4 timing edges per DUT cycle per channel. The function of each timing edge is described below.

Drive Format Capability

Channels programmed in QMM allow the most flexible formats including surround-by, clock and static drive formats.

Format	**Description**
SBC	Surround by Complement
SBCC	Surround by Complement, Complement
SBO	Surround by One
SBOC	Surround by One Complement
SBZ	Surround by Zero
SBZC	Surround by Zero Complement
SBT	Surround by Tri-State
SBTC	Surround by Tri-State Complement
NRZ	Non-Return to Zero
NRZC	Non-Return to Zero Complement
RZ	Return to Zero
RZC	Return to Zero Complement
RO	Return to One
ROC	Return to One Complement

Format	Description
RT	Return to Tri-State
RTC	Return to Tri-State Complement
RC/MANC	Return to Complement
RCC/MAN	Return to Complement, Complement
CLK	Clock High independent of pattern data
CLKC	Clock High Complement independent of pattern data
HI	Drive High independent of pattern data
LO	Drive Low independent of pattern data
OFF	Driver Tri-State independent of pattern data

Receive Format Capability

Format	Description
Strobe	Compare Edge Strobe
Window	Compare Window

Pass/Fail Generation

Compare	Description
High	Above Voh
Low	Below Vol
Midband	Below Voh and above Vol
Valid	Above Voh or below Vol
Mask	Don't compare

Timing Generators per Channel (DMM) 200 MVec/S

A channel configured in DMM has up to 2 timing edges per DUT cycle per channel. The 4 edges in a T0 cycle are configured to drive or compare 2 cycles of DUT data. The function of each timing edge is described below.

Drive Format Capability

Channels programmed in DMM support all Return-to, clock and static drive formats.

Format Name	Description
NRZ	Non-Return to Zero
NRZC	Non-Return to Zero Complement
RZ	Return to Zero
RZC	Return to Zero Complement
RO	Return to One
ROC	Return to One Complement
RT	Return to Tri-State
RTC	Return to Tri-State Complement
RC/MANCReturn to Complement	
RCC/MANReturn to Complement, Complement	
CLK	Clock High independent of pattern data
CLKC	Clock High Complement independent of pattern data
HI	Drive High independent of pattern data
LO	Drive Low independent of pattern data
OFF	Driver Tri-State independent of pattern data

Receive Format Capability

Format Name	Description
Strobe	Compare Edge Strobe
Window	Compare Window

Pass/Fail Generation

Compare	Description
High	Above Voh
Low	Below Vol
Midband	Below Voh and above Vol
Valid	Above Voh or below Vol
Mask	Don't compare

Timing Generators per Channel (SMM) 400 MVec/S

Channels operating in SMM are set to drive ONLY or compare ONLY. All 4 edges are used to drive data to the DUT or compare data from the DUT. A channel configured in SMM has 1 timing edge per DUT cycle per channel. The function of each timing edge is described below.

Drive Format Capability

Channels programmed in SMM support Non-Return and static drive formats.

Format Name	Description
NRZ	Non-Return to Zero
NRZC	Non-Return to Zero Complement
HI	Drive High independent of pattern data
LO	Drive Low independent of pattern data
OFF	Driver Tri-State independent of pattern data

Receive Format Capability

Format Name	Description
Strobe	Compare Edge Strobe

Pass/Fail Generation

Channels configured in SMM can support up to 4 of the 5 available compare states on-the-fly. A channel is statically configured to support either Midband or Valid.

Compare	Description
High	Above Voh
Low	Below Vol
Midband or Valid	Below Voh and above Vol Above Voh or below Vol
Mask	Don't compare

Edge Range

Minimum	*0 nS*
Maximum, the smaller of either	*2*(T0 Cycle) or 163.8 uS*

Edge Resolution

Edge resolution	*39.0625 pS*

Edge Placement Accuracy

Edge	
D0, D1, D2, D3 (drive edges)	*± 250 pS*
C0, C1, C2, C3 (compare edge strobe)	*± 250 pS*
Window Compare (min. glitch detection)	*1.25 nS*

Note: Edge placement accuracy applies at the DUT I/O connector of the test head when driving zero or one and comparing high or low at 3V. Timing accuracy does not apply for high voltage drivers.

SCAN Testing

Scan vector data and linear pattern data share the LVM. A SCAN channel's vector data is linked to 8 channels of LVM. Each DD48 card allows up to 3 independent SCAN chains where each SCAN chain has a SCAN IN and SCAN OUT channel. In addition, each SCAN IN and SCAN OUT channel can be connected to a maximum of 8 channels supporting multisite applications of SCAN chains allowing up to 24 SCAN IN and 24 SCAN OUT channels per DD48 card.

SCAN IN (Drive) Channel:

Pin State	Driver State
0	Low
1	High
X	Hiz

SCAN OUT (Compare) Channel:

Pin State	Compare Expect
0	Low
1	High
X	Mask

SCAN Memory Depth:

SCAN Chains	Vector Depth	SCAN IN Channels/ DD48	SCAN OUT Channels/ DD48	Max. SCAN Rate
3	1G	24 (max)	24 (max)	100 Mvps

Pattern Control

Cycle Counter

The 32 bit cycle counter contains the number of cycles executed by the pattern. Since the pattern can have repeat instructions, the number of vectors in a pattern and the number of cycles executed is often different.

Fail Counter

The 32 bit fail counter contains the number of failing cycles executed by a pattern.

History Ram

The 1K deep History Ram (HRAM) is used to capture the state of the system during pattern execution. The HRAM is used during pattern debugging. There are several modes of operation:

- Trigger on pattern label (address)
- Trigger on pattern cycle
- Capture all cycles or vectors
- Capture only failing cycles
- Capture the first 1K triggered cycles
- Capture the last 1K triggered cycles

Keep Alive Operation

Keep Alive operation is supported by allowing a pattern of any size to execute while modifying unused memory locations.

Waveform Send and Receive

Send and Receive Engine Architecture

Each DD48 pin card contains six 8-bit send and six 8-bit receive engines configured in send/receive engine pairs. Each send and receive engine pair has 128 Mb or memory per channel that can be used to source or capture serial or parallel data controlled by the digital pattern. The send and receive engine pairs can operate independently or with each other and can also be combined with other send and receive engine pairs to form larger parallel busses.

Each send and receive engine pair can support up to 256 unique segments, where each segment defines a send or receive data array of a user-defined size. This is useful for send functions that have different pre-defined waveforms (e.g. Sine or Cosine) or functions (e.g. DUT register reads and writes). The send and receive engines all support both QMM (100 MVec/S) and DMM (200 MVec/S) modes of operation.

The send and receive engines are generally useful for ADC and DAC testing, for general serial busses, and for DUT configuration register setup and testing.

Waveform Send and Receive Segments

Each send and receive engine pair has a 256 location shared segment table used to identify each data array by name and size. The content of the table can be used by pattern extended microcode to change from one data array to another. Switching from one data array to another is supported via extended microcode and may occur after the data array has finished or immediately via the STARTI/E and NEXTI/E extended micro-codes shown in the sections below.

Each send and receive engine pair has up to 128 M bits per channel of available data. Send and receive data arrays may utilize this memory up to the limit of the memory size with up to a combined total of 256 send and receive data arrays. The table below shows a few examples of serial and parallel vector sample sizes that may be stored or sent from each send and receive engine pair.

Serial or Parallel Mode	Number of Samples (Max.)
Serial, 8 bit	128 M samples
Serial, 16 bit	64 M samples
Parallel, up to 8 bits	128 M samples

Send/Receive Data rates

Extended micro-code execution speed is linked to the pattern sequencer vector rate. The maximum vector rate is 100 MVec/S. Each channel used for send or receive may be configured in either QMM or DMM, allowing data rates up to 100 MVec/S and 200 MVec/S, respectively.

Send Extended Microcode Instructions

STARTI	Start a new Send segment immediately
STARTE	Start a new Send segment after the current segment is finished
NEXTI	Get the next Send segment in the segment table and start it immediately
NEXTE	Get the next Send segment in the segment table and start it after the current segment is finished
SEND	Send a data sample to all configured channels
SHIFT	Shift a data sample serially to a configured channel
STOPI	Stop a current Send segment immediately
STOPE	Stop a current Send segment after the current segment is finished

Receive Extended Microcode Instructions

STARTI	Start a new Receive segment immediately
STARTE	Start a new Receive segment after the current segment is finished
NEXTI	Get the next Receive segment in the segment table and start it immediately
NEXTE	Get the next Receive segment in the segment table and start it after the current segment is finished
STORE	Receive a data sample on the configured channels
SHIFT	Shift a data sample serially from the configured channel

Programming

Drivers for C++, LabWindows™/CVI

Inherent support for multi-site, pattern and waveform editing and debugging.

SPECIFICATIONS

DIGITAL SUBSYSTEM SUMMARY

DD48 Overview

I/O per Board

48 digital channels

Date Rate:

Quad Marker Mode (QMM) 100 MVec/S

Dual Marker Mode (DMM) 200 MVec/S

Single Marker Mode (SMM) 400 MVec/S

Send/Capture Engines

1 per 8 channels

SCAN Pattern Engines

1 per 8 channels

PMU Measure ADC

1 per 8 channels

High Voltage Driver

1 per 8 channels

Mixed Signal Triggers

4 per board

Auxiliary Module Support

1 per board

Vector Memory

32 M Quad Marker Mode

64 M Dual Marker Mode

128 M Single Marker Mode

SCAN Pattern Memory

1G per Generator (Max)

Send and Capture Memory

128 M bits per channel shared between Send and Capture Engines.

1G serial (Max) per Engine

History Memory

1K

Micro Instructions

NOP, REP, HALT, LCNT, ENDL, JMP, JMPI, CJMP, JSR, CJSR, JSRI, RET, RCODE, HALT

Nested Subroutine Levels

16

Nested Loop Levels

16

T0 Period (Max)

671 mS with edge placement to 163.8 uS

Timing Sets

127 global

Edge Sets

32 per channel in QMM

Edge Placement Resolution

39.0625 pS

Edge Delay (Max)

163.8 uS

Edge Placement

0 to 2x period with no dead time

Timing Edges per Channel

4 flexible edges

Period Sets

32

Period Resolution

39 fs (10 ns/218)

Compare Formats

Strobe and Window

Drive Formats

NRZ, RZ, RO, RT, MAN, SBC, SBZ, SBO, SBT, CLK, HI, LO, OFF and their complements

CLK, HI, LO, OFF and their complements

DRIVER, COMPARATOR, LOAD (DCL)

Driver (3 Level Driver) plus High Voltage Driver

Voltage Levels

Driver Range	*-2.0 V to +6.0 V*
Vil	*-2.0 V to +5.9 V*
Vih	*-1.9 V to +6.0 V*
Vtt	*-2.0 V to +6.0 V*
Vhh	*+5.9 V to +12 V*

Comparator (Dual Level Comparator)

Voltage Levels

Comparator Range	*-2.0V to +6.0V*
Vol	*-2.0 V to +5.9 V*
Voh	*-1.9 V to +6.0 V*

Voltage Clamps

Voltage Levels

Clamp Range	*-2.0 V to +6.0 V*
Vclo	*-2.0 V to +5.0 V @ 1 mA*
Vchi	*-1.0 V to +6.0 V @ 1 mA*

Current Load

Current Levels

Current Range	*±12 mA*
Iol	*12 mA*
Ioh	*12 mA*

PER PIN PMU

PPMU FV/MI

Force Voltage Range

-2.0 V to +6.0 V

Measure Current Ranges

32 mA, 2 mA, 200 uA, 20 uA, 2 uA

PPMU FI/MV

Force Current Ranges

32 mA, 2 mA, 200 uA, 20 uA, 2 uA

Measure Voltage Range

-2.0 V to +6.0 V

Voltage Clamps

Clamp Range	*-2.0 V to +6.0 V*
Vcl	*-2.0 V to +4.0 V*
Vch	*-0.0 V to +6.0 V*

ACQUISITION MEMORY

PMU Acquisition Memory

Memory Depth

4 K Samples

Resolution

16 Bits

Sample Rate

100 Hz to 200 KHz, 1 uS resolution

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AEROFLEX
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Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused.

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